SERVICE MANUAL

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1827
FREQUENCY COUNTER

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I. INPUT SECTION (Fig. 1)

This is the most sensitive part of the unit, which is why a shield covers most of this section. The monolithic transistor package (IC 1) forms a differential amplifier and constant current source, regulated by the 4.3 volt zener, D2, and the series resistors R 10, R 12, and R 24.

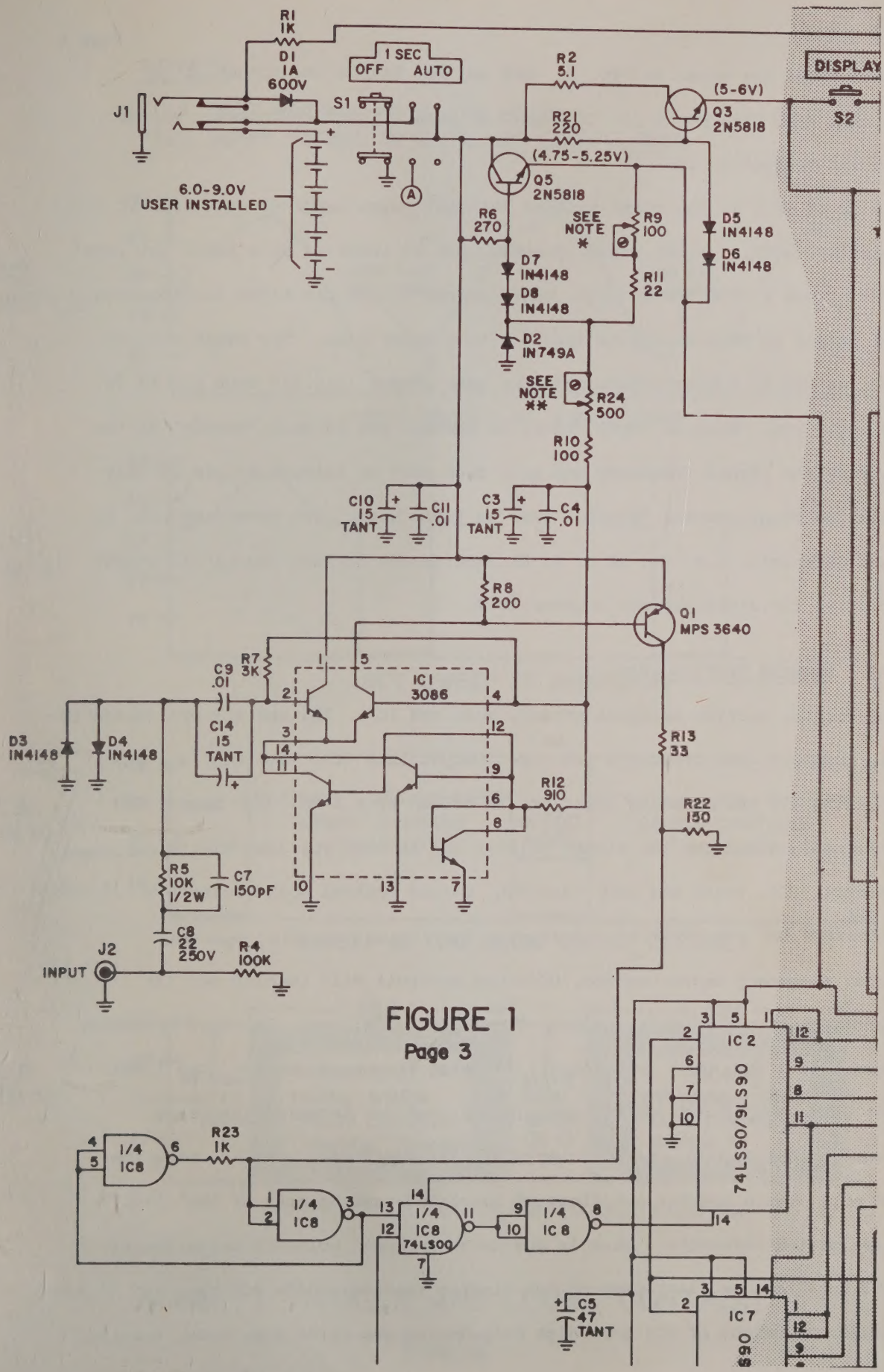
Capacitors C 10 and C 11 provide power supply filtering to IC 1 and transistor Q 1. C 3 and C 4 provide DC bias filtering (AC-signal ground) at differential input, pin 4 (IC 1). The bias at pin 4 (and at pin 2, due to bias resistor R7) is between 3 and 3.5 volts depending upon setting of R 24.

Diodes D3 and D4 protect IC 1 and the AC-coupling capacitors, C9 and C 14, from excessive voltage by limiting the peak AC signal voltage to only one diode drop (.7 volt) above and below ground. R5 protects D1 and D2 from excessive current whenever they are driven into forward conduction by the signal. Compensation capacitor C7 improves the high frequency response of the protection circuit. R4, along with D3 and D4, provide the discharge path for the DC-blocking capacitor C8.

The output driver transistor, Q1, is biased by the voltage drop across R8, and thus is dependent upon the bias current through IC 1. Adjustment of R24 therefore sets-up the bias for both IC 1 and Q1. R24 is adjusted so that 2 volts is present at pins 1 and 2 of IC 8 (Unit operating at 6V. See CALIBRATION). This is the guarenteed minimum logic high for the low power schottky nand gate (IC8). If a logic high is not present at pins 1 and 2 of IC8, then a "1" count will always be displayed (000.001 KHZ) instead of a "Zero" count (000.000 KHz) when no input signal is present.

II. SCHMITT TRIGGER AND COUNT CONTROL SECTION (FIG. 1)

The Schmitt trigger circuit consists of two (2) nand gates (IC8, pins 1-6) and R23, connected in a positive feedback arrangement. Waveforms seen at


R1
1K
D1
1A
600V
1 SEC
OFF AUTO
S1
J1
R2
5.1
(5-6V)
Q3
2N5818
R21
220
DISPLAY
S2
(4.75-5.25V)
Q5
2N5818
6.0-9.0V
USER INSTALLED
R6
270
SEE
NOTE
*
R9
100
D5
IN4148
D6
IN4148
D7
IN4148
D8
IN4148
R11
22
D2
IN749A
SEE
NOTE
**
R24
500
R10
100
C10
15
TANT
C11
.01
C3
15
TANT
C4
.01
R8
200
Q1
MPS 3640
R7
3K
C9
.01
IC1
3086
D3
IN4148
D4
IN4148
C14
15
TANT
R13
33
R12
910
R22
150
R5
10K
1/2W
C7
150pF
C8
22
250V
J2
INPUT
R4
100K
FIGURE 1
Page 3
R23
1K
1/4
IC8
74LS00
IC 2
74LS90/9LS90
C5
47
TANT
IC 7
690

these gates are shown in FIG. 2. R13 and R22 divide the output of Q1 so that some hysteresis is introduced at pins 1 and 2 of IC 8 due to the schmitt trigger action.

Pin 12 of IC 8 is the count control "window" pulse input (coming from IC 3). Normally, with no input signal present, pin 13 (IC8) is at a logic low level [pins 1 and 2 (IC8) are at logic high, so pin 3 (and pin 13) is low], forcing the output of this nand gate (pin 11) to a logic high. The count control (CC) at pin 12 has no affect upon the gate output (pin 11) when pin 13 is at logic low. When an input signal is present pin 13 will "toggle" at the rate of the signal frequency and will then pass on through to pin 11 only when the count control "window" goes to logic high. See waveforms FIG. 2. Nand gate (pins 8,9, and 10 of IC 8) inverts and buffers the pin 11 output to drive the divide-by-ten counter IC 2.

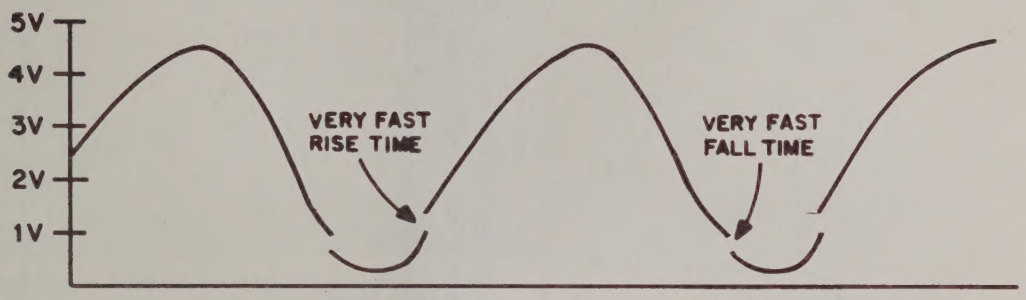
III. COUNTER SECTION (FIG. 3)

The counter section consists of IC2, IC3, and IC7. IC2 and IC7 are divide-by-ten counters that produce a BCD coded output into IC3. See FIG. 4. IC3 contains all the counting logic and is driven by a 1 MHZ time base. IC3 internally develops the strobe pulses, DS1 through DS6 (See FIG.5), the count control (CC), reset out (RO) (See FIG. 6) and decimal point select(DP1,2 and 3) necessary for the counting and display functions. Depending upon the input frequency being counted, CC(count control) will go high for (3) different time period intervals. These are as follows: Incoming frequency less than 1 MHZ, CC=1 sec. (high); incoming frequency greater than 1 MHZ but less than 10 MHZ, CC=100 msec (high); and for incoming frequency greater than 10 MHZ, CC=10msec (high). See waveforms, FIG.6. Note that CC must remain low for a minimum of about 200 msec in each of the (3)CC time period intervals. This is due to an internal hold-off delay timing in IC3 to eliminate flickering of the display reading in the 100 msec and 10 msec modes.DP1 output of IC3 goes high only during the CC=10 msec mode, turning

NOTES:

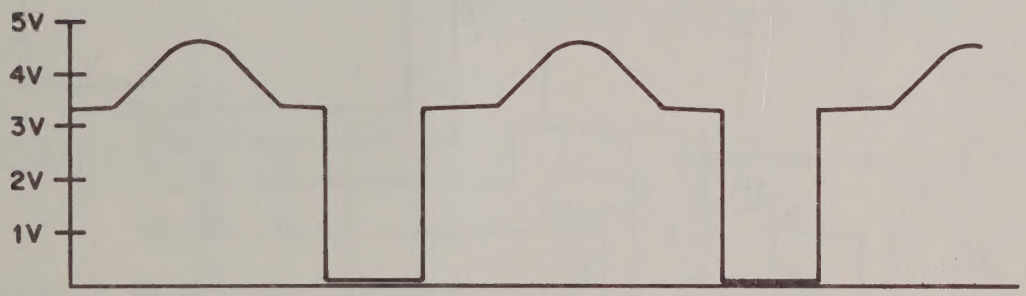
(1) UNIT OPERATING AT 7.5 VOLTS.
(2) INPUT SIGNAL IS 100Hz. AT 200mV. RMS.

IC8 PINS 1,2



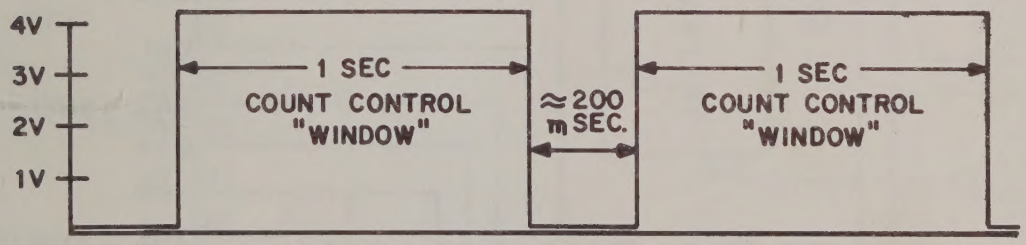
SET SWEEP AT 2 mSEC/DIV

IC8 PIN 6



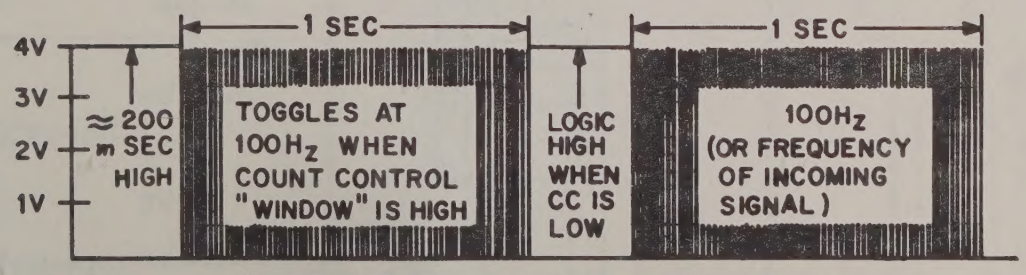
SET SWEEP AT 2mSEC/DIV

IC8 PIN 12



SWEEP IS TOO SLOW TO SEE CLEARLY

IC8 PIN 11



SWEEP IS TOO SLOW TO SEE CLEARLY

SCHMITT TRIGGER AND COUNT CONTROL

FIG. 2

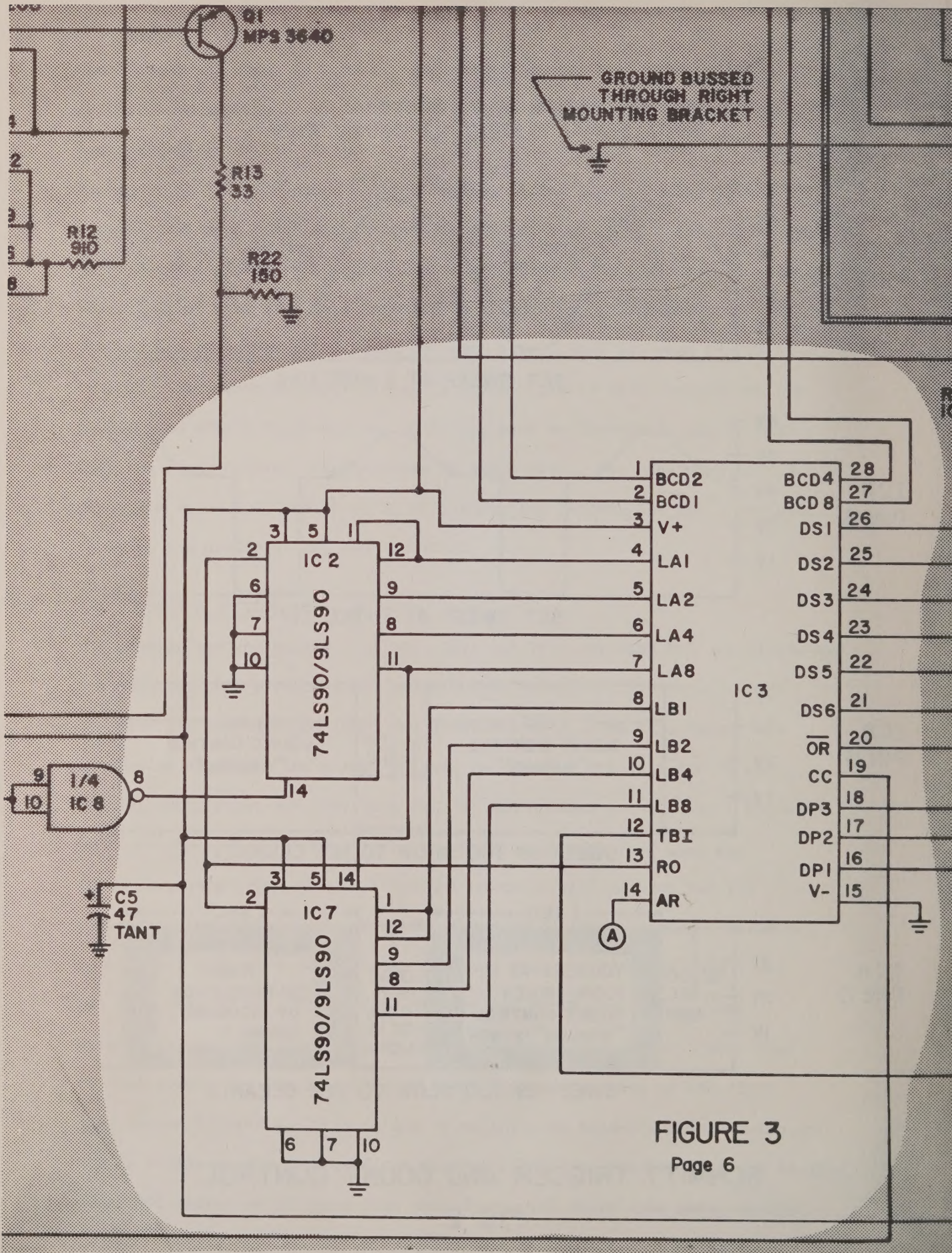
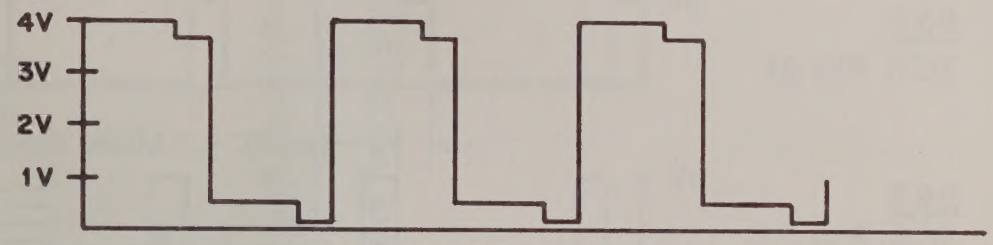

Q1
MPS 3640
GROUND BUSSED
THROUGH RIGHT
MOUNTING BRACKET
R13
33
R12
910
R22
150
IC 2
74LS90/9LS90
1/4
IC 8
C5
47
TANT
IC 7
74LS90/9LS90
IC 3
BCD2
BCD1
V+
LA1
LA2
LA4
LA8
LB1
LB2
LB4
LB8
TBI
RO
AR
BCD4
BCD 8
DS1
DS2
DS3
DS4
DS5
DS6
OR
CC
DP3
DP2
DP1
V-

FIGURE 3

NOTES:

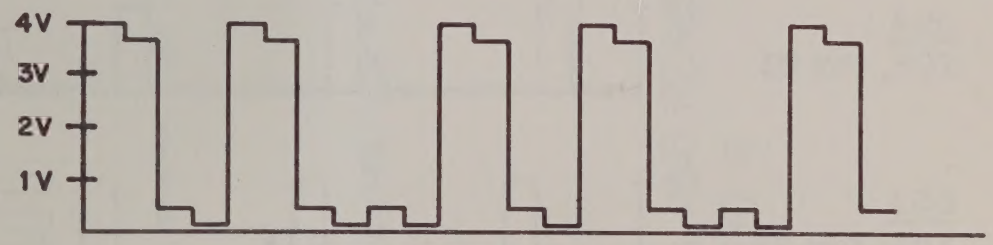
(1) WAVEFORMS LA1, 2, 4 AND 8 WITH INPUT SIGNAL AT 100Hz.
(2) WAVEFORMS LB1, 2, 4 AND 8 WITH INPUT SIGNAL AT 1KHz.
(3) WAVEFORMS PRESENT ONLY WHEN COUNT CONTROL (CC) IS HIGH; WHEN CC IS LOW, STATE IS EITHER HIGH OR LOW.

LA1
IC3, PIN 4 (100Hz.)
AND
LB1
IC3, PIN8 (1KHz.)



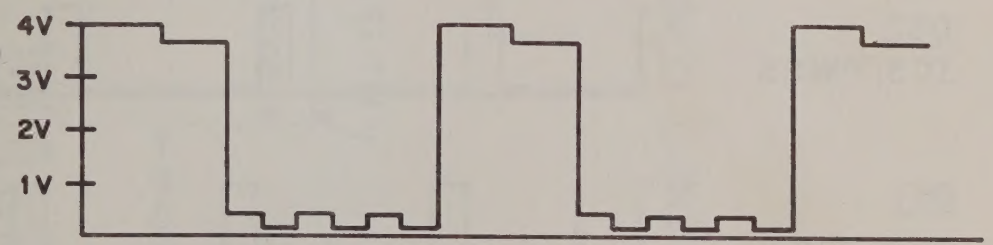
SET SWEEP AT 5mSEC/DIV

LA2
IC3, PIN 5 (100Hz.)
AND
LB2
IC3, PIN9 (1KHz.)



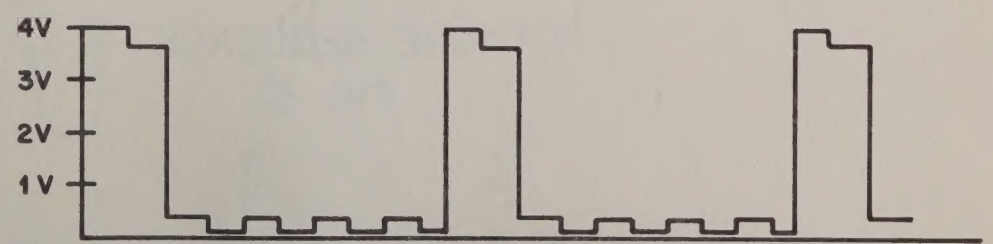
SET SWEEP AT 20mSEC/DIV

LA4
IC3, PIN6 (100Hz.)
AND
LB4
IC3, PIN 10 (1KHz.)



SET SWEEP AT 20mSEC/DIV

LA 8
IC3, PIN 7 (100Hz.)
AND
LB8
IC3, PIN 11 (1KHz.)

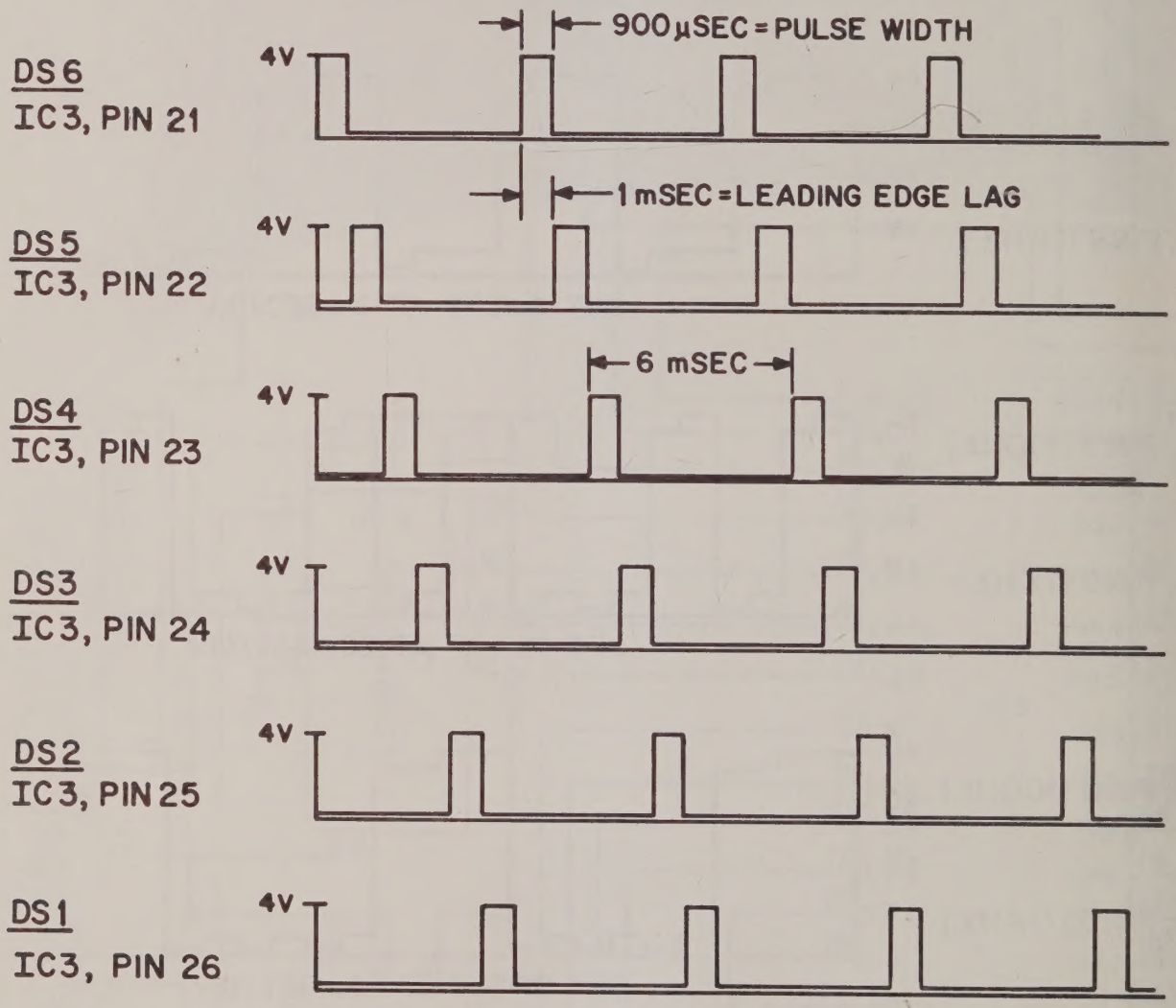


SET SWEEP AT 20mSEC/DIV

COUNTER SECTION
FIG. 4

NOTE:

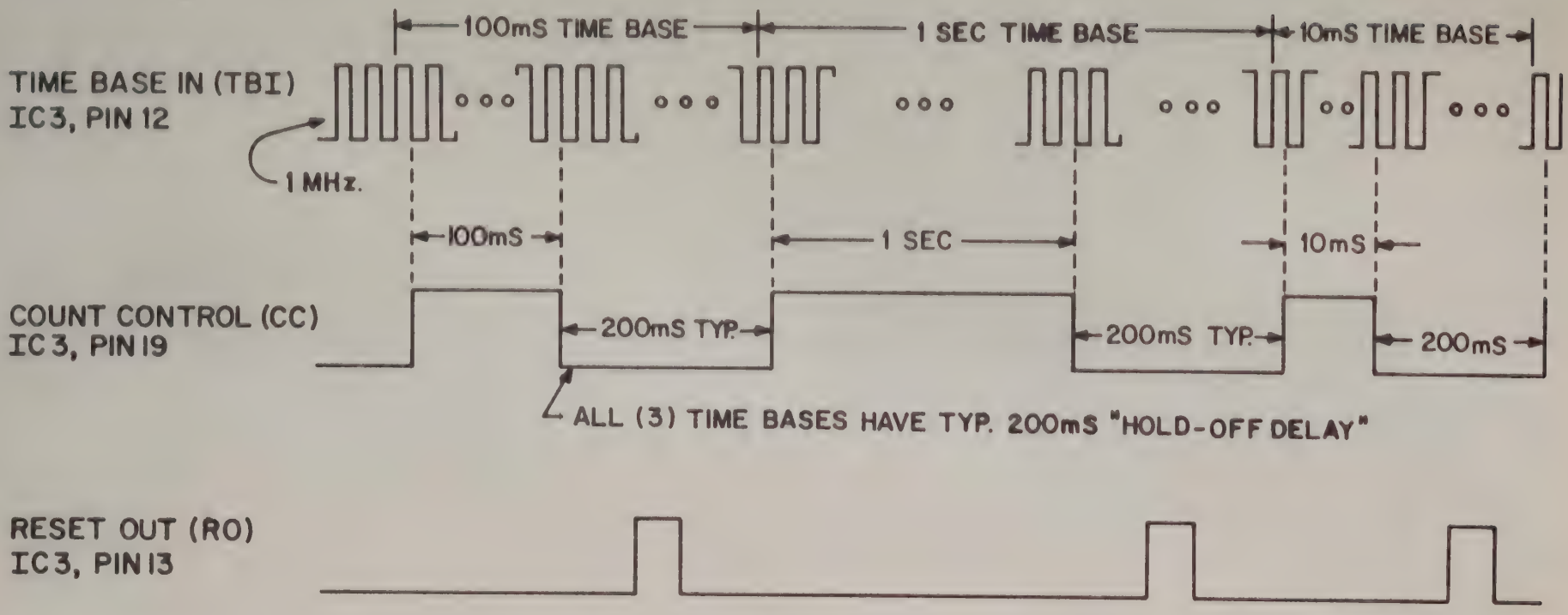
DS6 (DS101) IS THE MOST SIGNIFICANT DIGIT (MSD) AND
DS1 (DS106) IS THE LEAST SIGNIFICANT DIGIT (LSD).



STROBE SEQUENCE
FIG. 5

NOTE:

THREE SEPARATE TIME BASES GENERATED BY IC3 DEPENDING UPON INCOMING FREQUENCY (AUTO. SW. POS.).



COUNT CONTROL AND RESET OUT

FIG. 6

on the appropriate decimal point. Likewise, DP2 goes high during the CC=1 sec mode and DP3 goes high only during the CC=100 msec mode. Therefore, only one decimal point can be on at any one time.

IV. TIME BASE SECTION (FIG.7)

A 4 MHZ crystal controlled oscillator is the heart of the frequency counter. The oscillator circuit is temperature compensated to have a zero temperature coefficient and any variation in frequency is due to the crystal itself ($\pm$ 10 ppm from $0^{o}C$ to $50^{o}C$). IC6 takes the output of the 4 MHZ oscillator and divides it by 4 (two (2) "D-type" Flip Flops, each dividing by 2) for a 1 MHZ time base required by IC3. See waveforms FIG. 8.

V. DISPLAY SECTION (FIG. 9)

The output of IC3 is multiplexed. BCD1,2,4 and 8 (IC3, pins 1, 2, 27, and 28) are the BCD outputs and are decoded by IC 101 into seven segment outputs that drive, in parallel, digits DS101 through DS106, current limited by resistors R102-R108. DS1 through DS6 (IC3, pins 21-26) are the strobed outputs that are inverted and buffered by IC4, and sink the digit segments. See waveforms, FIG.10.

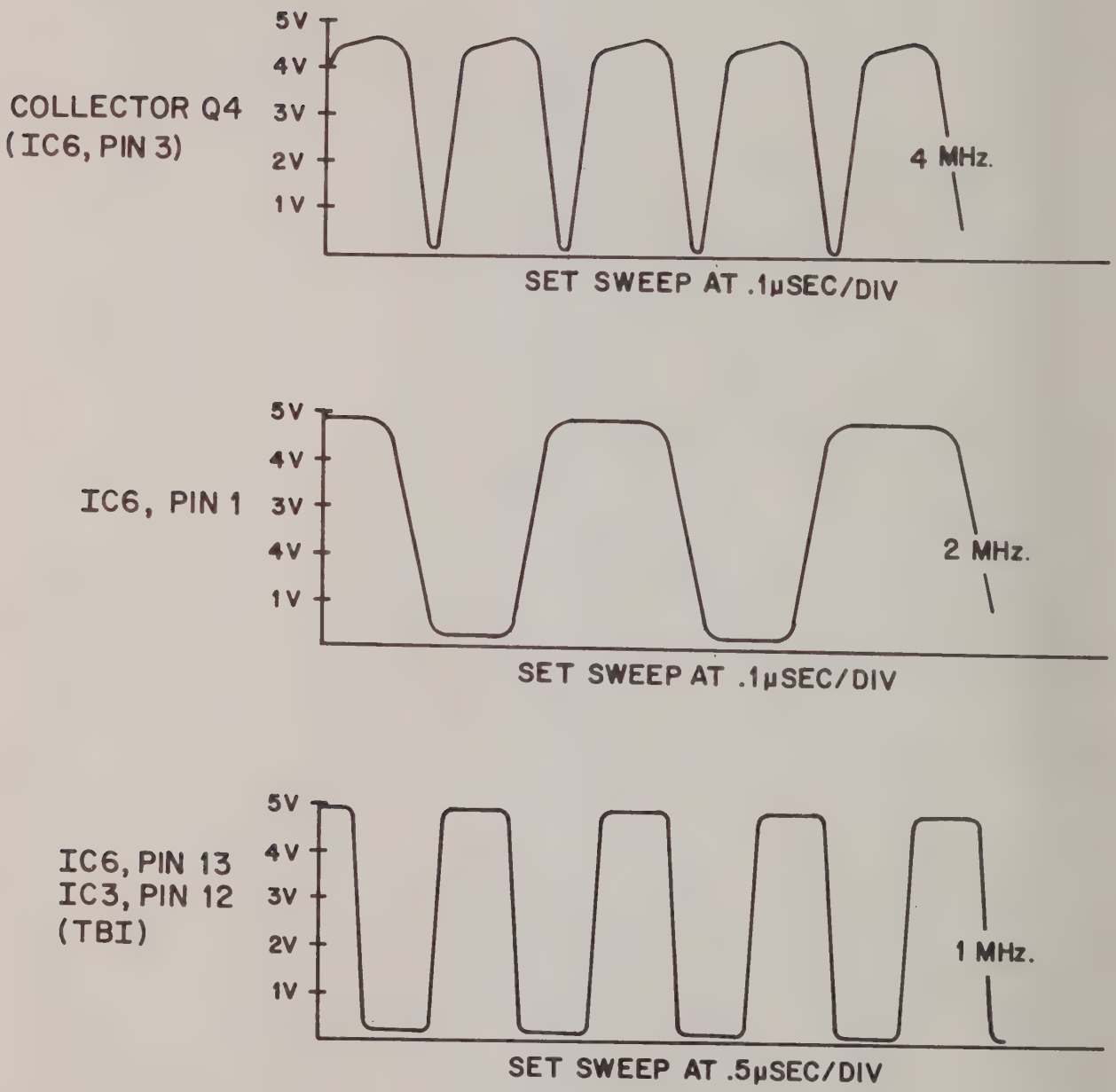
Resistor R109 and capacitor C101 provide a R-C time constant voltage discharge at the $\overline{BI}$ (blanking) input of IC101 (pin 4). When DISPLAY switch S2 is pushed, C101 is charged through R3 to near the Q3 emitter voltage. When S2 is released, C101 will discharge through R109 and when the voltage at $\overline{BI}$ reaches approximately 1/3 of the Q3 emitter voltage, the display digits will blank (approximately 8-10 sec.). When the unit is externally powered, through jack J1, C101 will charge to the Q3 emitter voltage +.7 volt (diode clamped in IC101) and the displays will stay on continuously.

VI. DECIMAL POINT AND KHZ/MHZ CIRCUIT (FIG.9)

The three decimal point outputs, DP1,2, and 3 of IC3 turn on the appropriate decimal point and select the KHZ/MHZ indicators. When DP2 goes high

3401
IC4
75492
IC3
IC2
74LS90/9LS90
IC7
74LS90/9LS90
Q4
MPS2369
X1
4MHz
R14
10K
R18
100
R20
270
R17
22K
R18
47K
R19
470
R22
150
C16
.01
C17
47
TANT
C13
30pF
N750
C12
2-10pF
C15
150pF
N750
C18
47
TANT
OVER

FIGURE 7



TIME BASE WAVEFORMS
FIG. 8

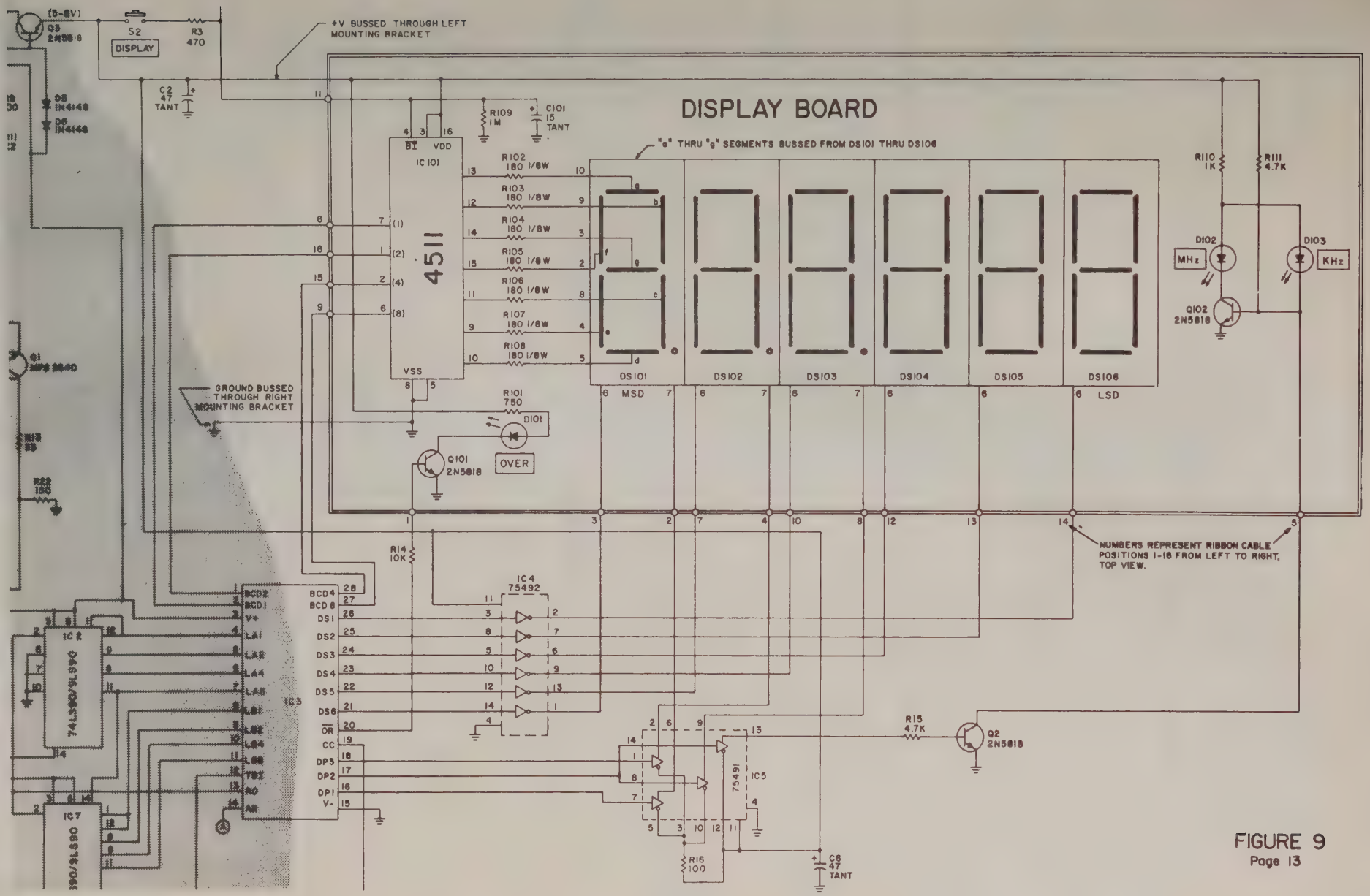


FIGURE 9
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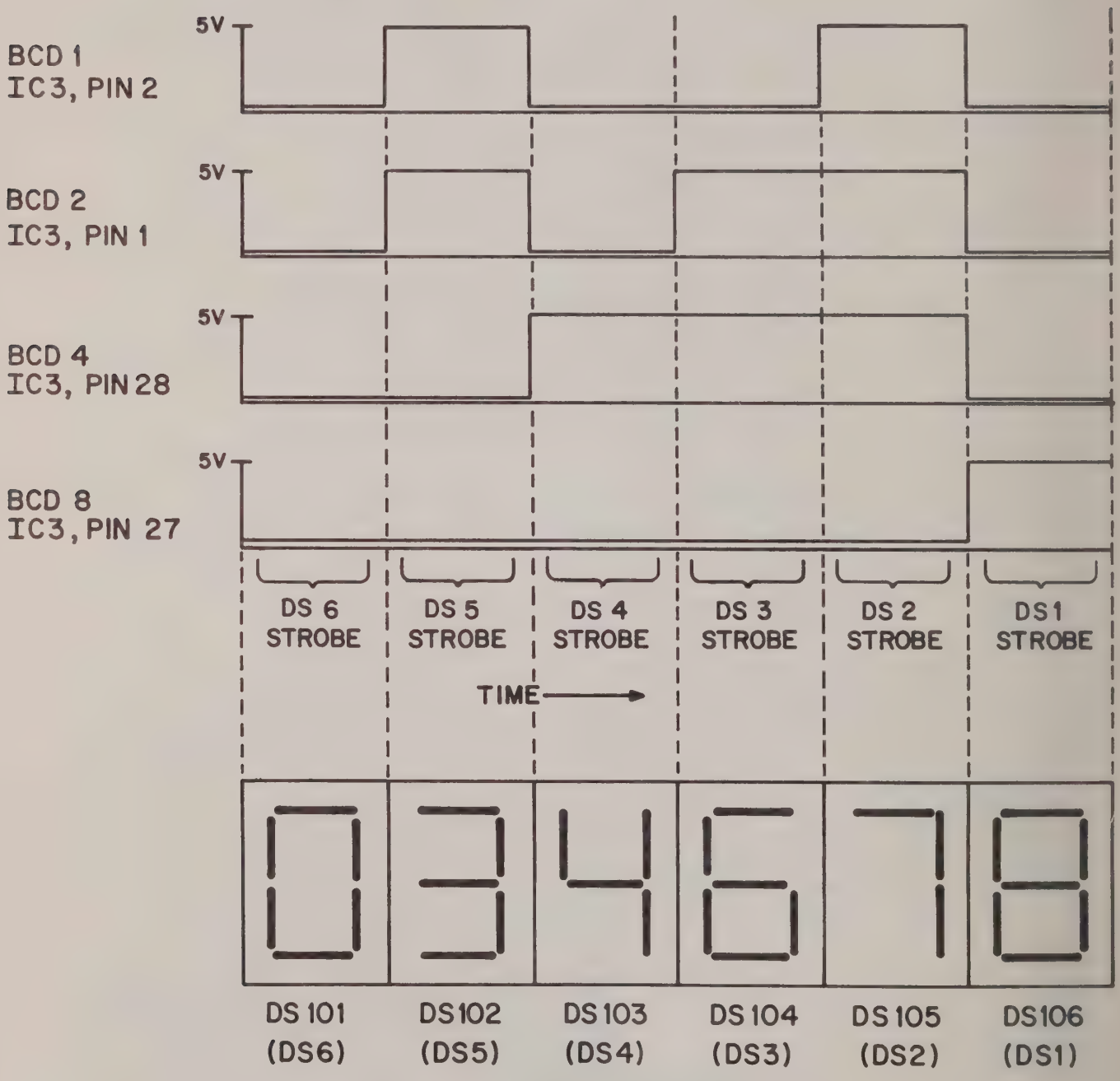
EXAMPLE:

BCD 1, 2, 4 AND 8 OUTPUTS CORRESPONDING TO NUMERICAL FIGURES DISPLAYED.



EXAMPLE OF BCD MULTIPLEXED DISPLAY

FIG. 10

(DP1 and DP3 are both low), the KHZ LED (D103) will light. When DP2 goes low (DP1 or DP3 is high), the MHZ LED (D102) will light. IC5 is a non-inverting buffer to drive the decimal point segments. Each of DP1, 2, and 3 turn on a separate decimal point. Transistor Q2 goes into saturation when DP2 goes high and therefore turns on KHZ LED D103 and turns off transistor Q102 and MHZ LED D102. When DP2 goes low transistor Q2 is turned off, KHZ LED D103 is turned off, and transistor Q102 and MHZ LED D102 are turned on.

VII. POWER SUPPLY SECTION (FIG. 1)

Q3 and Q5 are voltage regulating transistors that allow the frequency counter to operate over the 6 to 9V range. Zener diode, D2, besides regulating the input section, also limits the voltage regulation of Q5 to ±.25V. Diodes D7 and D8 in series with D2 set the base voltage of Q5 at the appropriate value (≃5.45V) to give 4.75V at the emitter of Q5 when 6V is applied at the collector of Q5 (supply Voltage). R6 forward biases D7 and D8 each at about .65V and D2 will be at approximately 4.15V. Adjust R9 to set the voltage of D2 to give 4.75V at emitter of Q5 (See Calibration, below). The base of Q3 is clamped by D5 and D6 so that the bias can be no greater than two diode drops above the emitter of Q5. This limits the voltage at the emitter of Q3 to less than 6V when 9V is present at the collector of Q5. R21 provides a current by-pass so that when D5 and D6 are not conducting, the emitter of Q3 sits at .7V less than the collector of Q3. Therefore, at 6V unit operation (6V at collector of Q5), the emitter of Q3 will be 5.25V or greater. R2 helps filter out the noise generated by the display circuitry powered by Q3. At 9V unit operation the emitter of Q5 should be less than 5.3V.

VIII. SERVICE AND CALIBRATION

To service the unit, remove the 4 screws at the bottom of the case and remove the top cover. Observe proper polarity when installing new batteries. See FIG. 11. Location of adjustment points are shown also

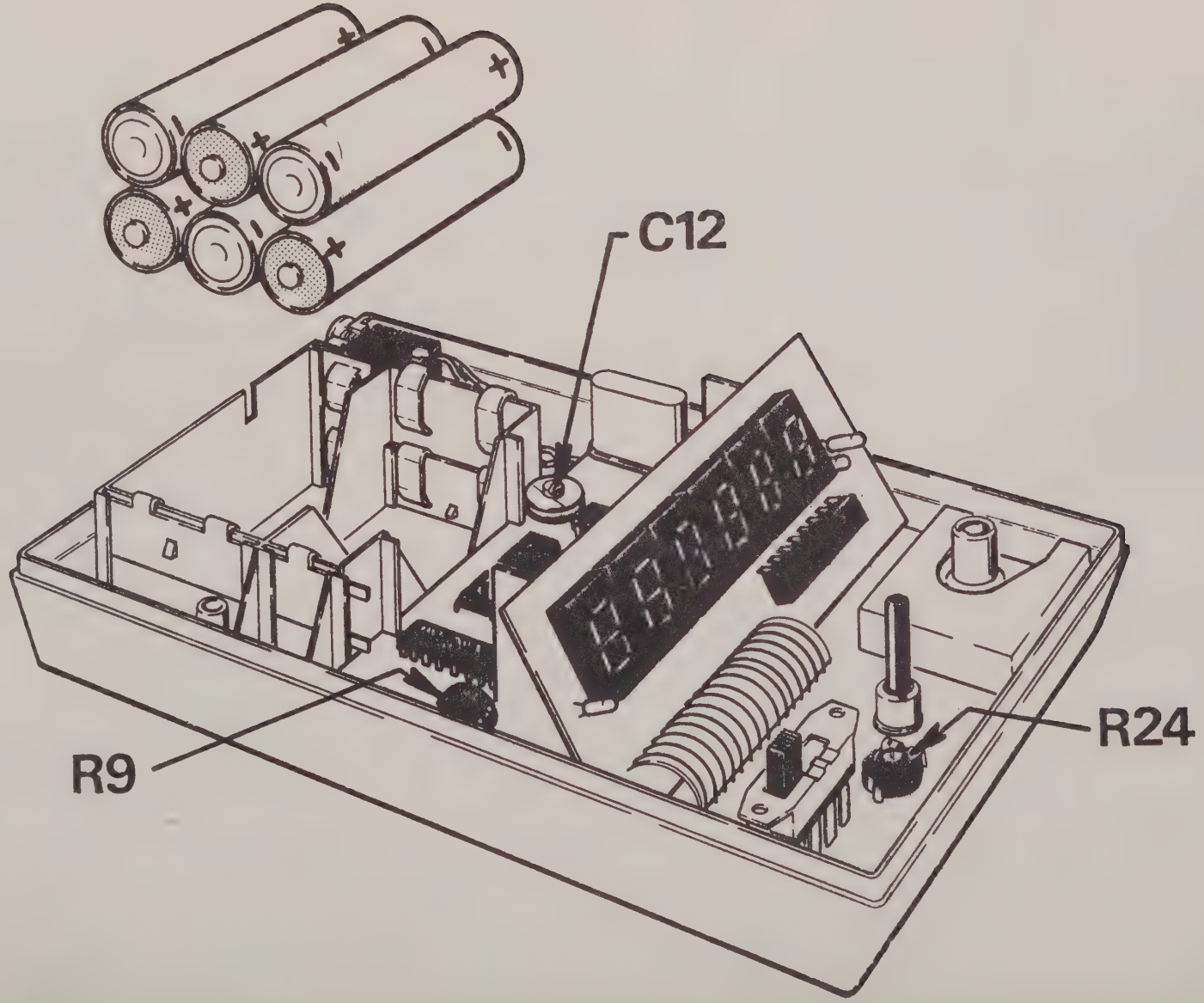


FIG. 11

SERVICE AND CALIBRATION

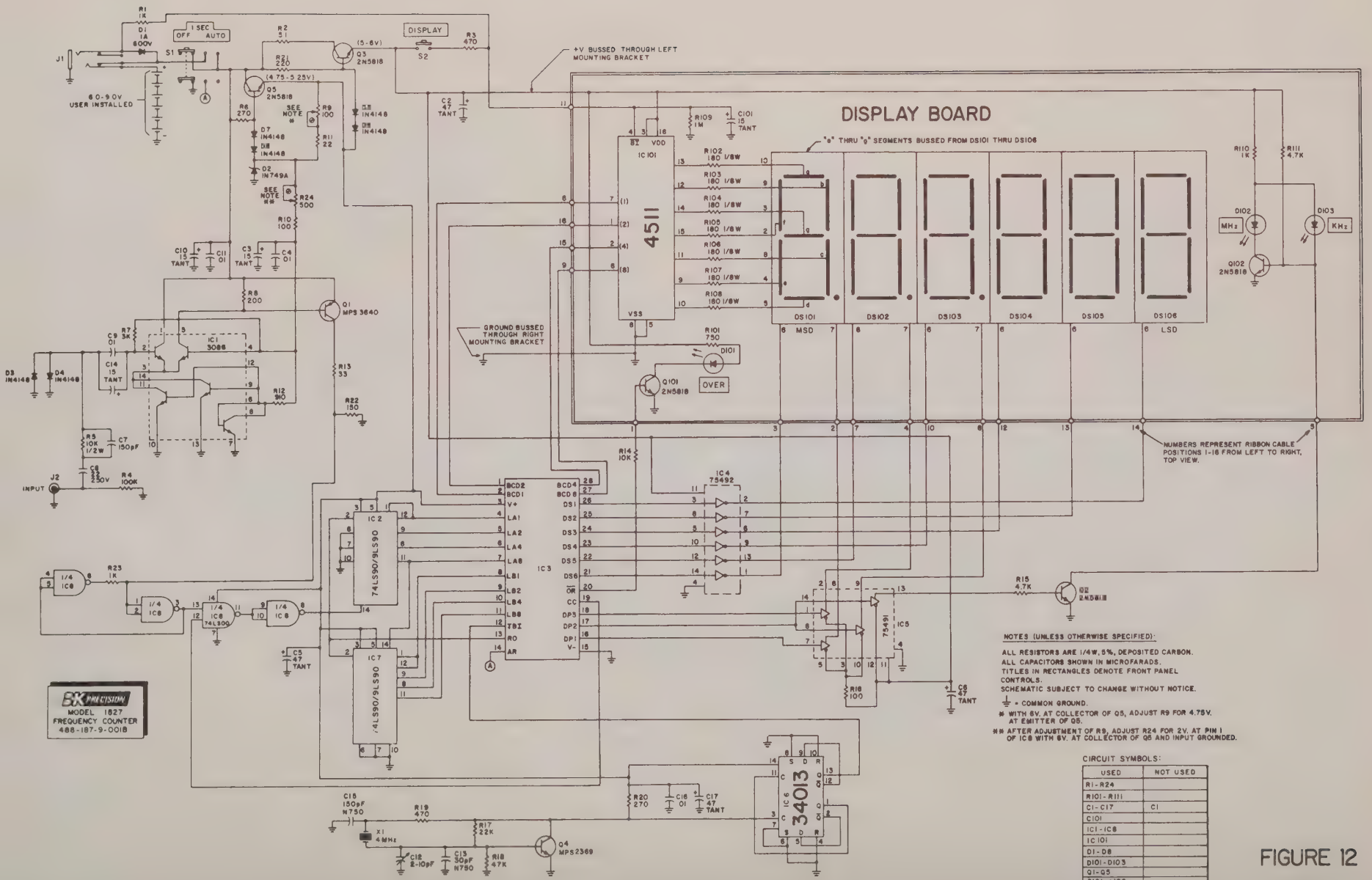
in FIG.11.

To calibrate the oscillator, a 10 MHz standard with accuracy of at least ±1 part in 10^8 is required to set the oscillator ±1 HZ of 10 MHZ (a 1 MHz standard can be used to set the oscillator ±10 Hz of 10 MHz).

PROCEDURE:

1. Adjust R9 so that the emitter of Q5 measures 4.75 volts with 6 volts applied at the collector of Q5.
2. Adjust R24 so that Pin 1 of IC8 measures 2 volts with 6 volts applied at the collector of Q5 and no input signal.
3. Place unit at room ambient temperature, unless a more specific temperature is required for the temperature at which your frequency counter is most often used. See SPECIFICATIONS for frequency stability.
4. Connect the standard frequency source to the input jack.
5. Operate unit near the center of the voltage operating range (7.5 volts) or use optional AC adapter BC-27.
6. Set function switch to "1 SEC" position.

   NOTE: The instrument will overrange and the most significant digits will be lost.
7. With a non-metallic alignment tool, adjust C12 for display reading equal to the standard frequency ±1 count.



NOTES (UNLESS OTHERWISE SPECIFIED):

ALL RESISTORS ARE 1/4W, 5%, DEPOSITED CARBON.
ALL CAPACITORS SHOWN IN MICROFARADS.
TITLES IN RECTANGLES DENOTE FRONT PANEL CONTROLS.
SCHEMATIC SUBJECT TO CHANGE WITHOUT NOTICE.
⏚ = COMMON GROUND.
* WITH 8V. AT COLLECTOR OF Q5, ADJUST R9 FOR 4.75V. AT EMITTER OF Q5.
** AFTER ADJUSTMENT OF R9, ADJUST R24 FOR 2V. AT PIN 1 OF IC8 WITH 8V. AT COLLECTOR OF Q5 AND INPUT GROUNDED.

CIRCUIT SYMBOLS:

USED	NOT USED
R1-R24	
R101-R111	
C1-C17	C1
C101	
IC1-IC8	
IC 101	
D1-D8	
D101-D103	
Q1-Q5	
Q101-Q102	

FIGURE 12

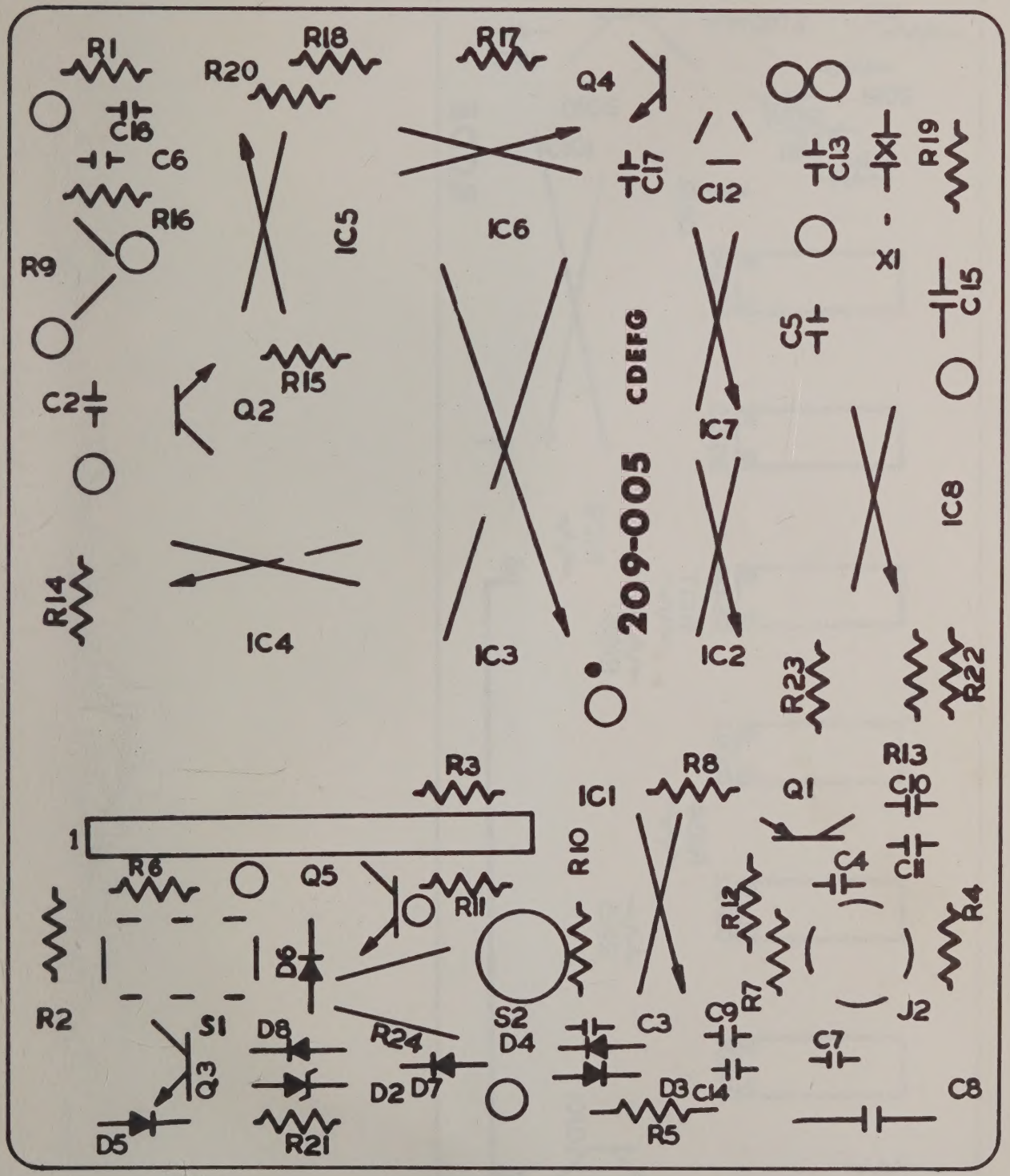


FIGURE 13
PARTS LAYOUT MAIN PCB
COMPONENT SIDE

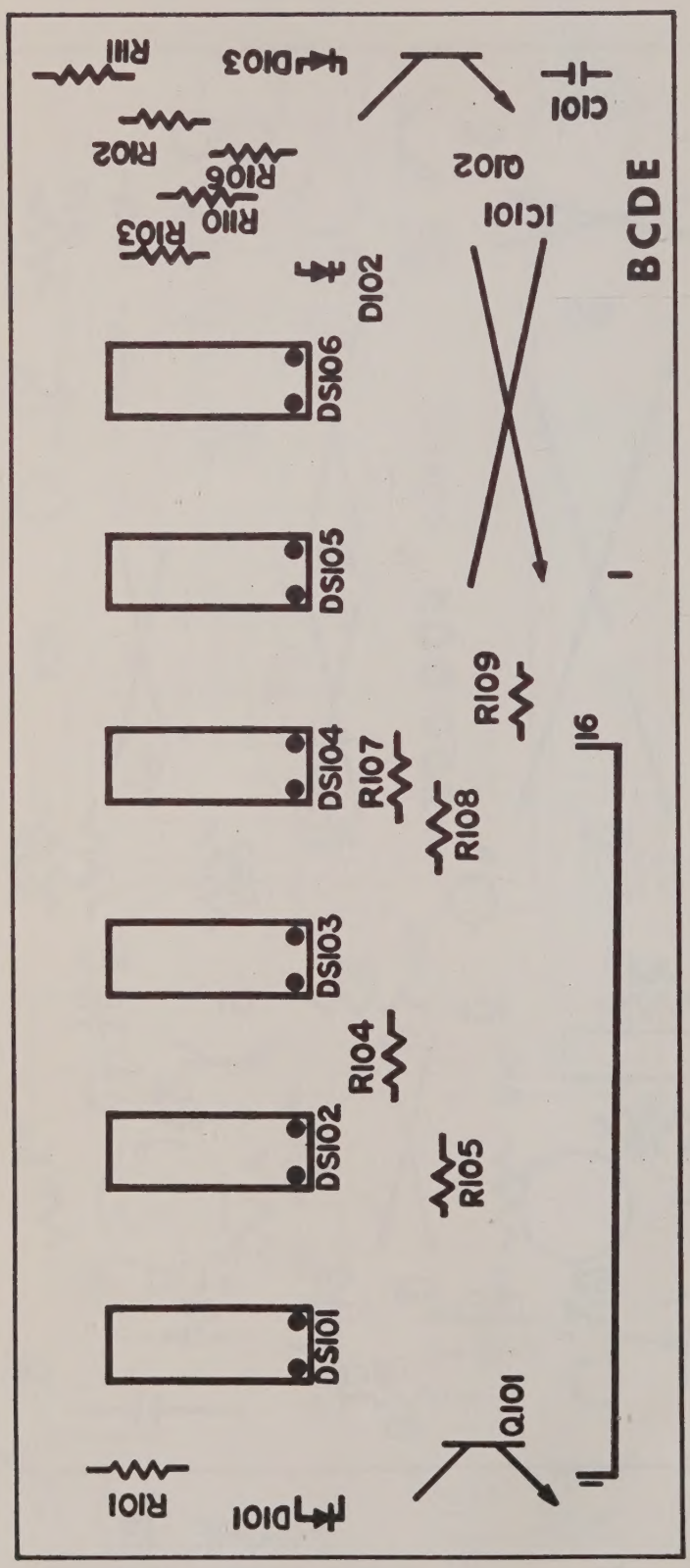


FIGURE 14
PARTS LAYOUT DISPLAY PCB
COMPONTNENT SIDE